CMOS ISOLATION CELL FOR EMBEDDED MEMORY IN POWER FAILURE ENVIRONMENTS

ABSTRACT

An embedded memory on an integrated circuit chip is capable of being isolated from other on chip and off chip circuitry during power failure modes on the integrated circuit chip. The embedded memory preferably has its own external power supply. When power on chip fails or falls below a threshold level, input to and output from the embedded memory is prohibited by CMOS isolation cells. The CMOS isolation cells are controlled by enable signals and the power level of other power supplies within the integrated circuit.